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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,423	06/30/2003	Zurab Khasidashvili	INTEL-0022	8079

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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,423	KHASIDASHVILI ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-27* is/are pending in the application, wherein claims 1-5 are canceled.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-25 and 27* is/are allowed.

6)☐ Claim(s) *6-8 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Applicant's amendment filed on 1/6/2006. Claims 6-27 are pending, wherein claims 1-5 have been canceled, claims 6-7,9,12,16,19-20,22 have been amended, and claims 25-27 have been newly added. Claims 6-27 have been examined. As per **claims 6-8,26**, Applicant's arguments are not persuasive; therefore the previous Office Action is incorporated herein. As per **claims 9-25,27**, the claims are allowed.

Drawings

2. As previously indicated, the drawings were received on 11/14/2003. These drawings are approved by the Examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 6-8,26** are rejected under 35 U.S.C. 102(b) as being anticipated by **Bischoff et al.** ("Formal Implementation Verification of the Bus Interface Unit for the Alpha 21264 Microprocessor", Proceedings of the 1997 IEEE International Conference on Computer Design: VLSI Computers and Processors, 12 October 1997, pp. 16-24).

As per **claims 6,26**, the formal equivalence verification is discussed in the abstract (page 16), wherein the computation of the Timed Binary Expression Diagram

(TBED) is illustrated in Fig. 3, as part of the TTBDD (see page 19) based on the BDD (i.e., Boolean formula) since Applicant's specification does not clearly define what BED (Binary Expression Diagram) is, the use of the expression out=in [!clk, clk] as described on page 19, col. 1, are also equivalent to the exemplary BED expression as discussed in Applicant's specification, pages 5-6, and the Timed Ternary BDD (TTBDD) would accordingly corresponds to the TBED, as claimed; wherein the applying to the SAT solver or BDD tool to establish equivalent is part of the applying to the BOVE (page 19, col. 1, paragraph 2; sections 4 and 5).

As per **claim 7**, all of the elements of claim 6, from which the claim depends, are discussed in the rejection of claim 6 above, wherein the further comparison of the TBEDs (i.e., TBDDs) of a specification circuit (i.e., schematic) and an implementation circuit (i.e., RTL) is also described in section 5, page 18.

As per **claim 8**, all of the elements of claim 7, from which the claim depends, are discussed in the rejection of claim 6 above, wherein the circuit is pipelined circuit (i.e., part of the pipeline stages) as discussed in the abstract and further the circuit is further loop-free as describe in section 4.1 (page 18) in which the combinational loops are converted to the equivalent latch or combinational logic, for which the verification applies.

Allowable Subject Matter

5. **Claims 9-25,27** are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter:

7. As per **claims 9-25,27**, the Office Action mailed on 10/6/2005 sets forth the patentability of Applicant's claimed invention, wherein as previously indicated, the independent claims 9, 20,22, from which the claims depend respectively, recite the method/system/computer readable media comprising the inventive steps/means/code for listing/placing the latches in a predetermined order in combination with the representing and computing steps/means/code as claimed, which corresponds to Applicant's specification, paragraph [14], page 4 to paragraph [51], page 14, (see especially page 11, paragraph [41]), which the prior arts made of record failed to teach or suggest. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Remarks

8. The objections of **claims 4-24** are due to the noted informalities are withdrawn in light of Applicant's amendment filed on 1/6/2006, which corrected the informalities and rendered the informalities muted as per claims 4-5 due to the cancellation of claims 4-5.

9. As per **claims 6-8,26**, Applicant argued that **Bischoff** does not teach computing a Timed Binary Expression Diagram (TBED) for each circuit node but rather merely discloses the use of Binary Decision Diagrams (BDDs) such as Ternary Binary Decision Diagrams (TBDDs), and not a TBED (see Applicant's amendment, page 8). The Examiner is not persuaded. As noted in the previous rejection of the claims and incorporated herein above, Applicant's specification does not clearly define what is meant by Timed Binary Expression Diagram. Since the BED (Binary Expression Diagram) refers to the graphical representation of the Boolean expression (Boolean

formula) as pointed out by Applicant (see paragraph [30] of Applicant's specification and page 7 of Amendment filed on 1/6/2006), the BDD (Binary Decision Diagrams) is considered an equivalent BED since it also meets this definition. Furthermore, the Timed Ternary Binary Decision Diagram (TTBDD) as used herein is also equivalent to the TBED, since this TTBDD is also computed from the equivalent BED (i.e., BDD), having timing (i.e., clock) component as discussed in the rejections of claims 6,26 above. Accordingly, the application of the SAT solver or BDD tool, operating on these equivalent TBEDs (i.e., TTBDD) is also taught by **Bischoff**.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is herein requested to consider them carefully in response to this Office Action. In particular, the following prior arts made of record are most relevant:

Prasad et al. (U.S. Patent Application Publication No. 2004/0237057, especially paragraphs [0017]-[0018], [0028]-[0029]);

Jain (U.S. Patent Application Publication No. 2004/0098682, especially paragraphs [0006], [0024], [0101]);

Burch et al. (U.S. Patent No. 6,247,163, especially col. 2, lines 51-63; col. 5, lines 52-61; col. 9, line 24 to col. 10, line 10).

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 6:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

Phallaka Kik
U.S. Patent Examiner
February 8, 2006